

2. MIKROPROCESOR 8086

Centralna procesorska jedinica

(CPU - “*central processing unit*”) sadrži:

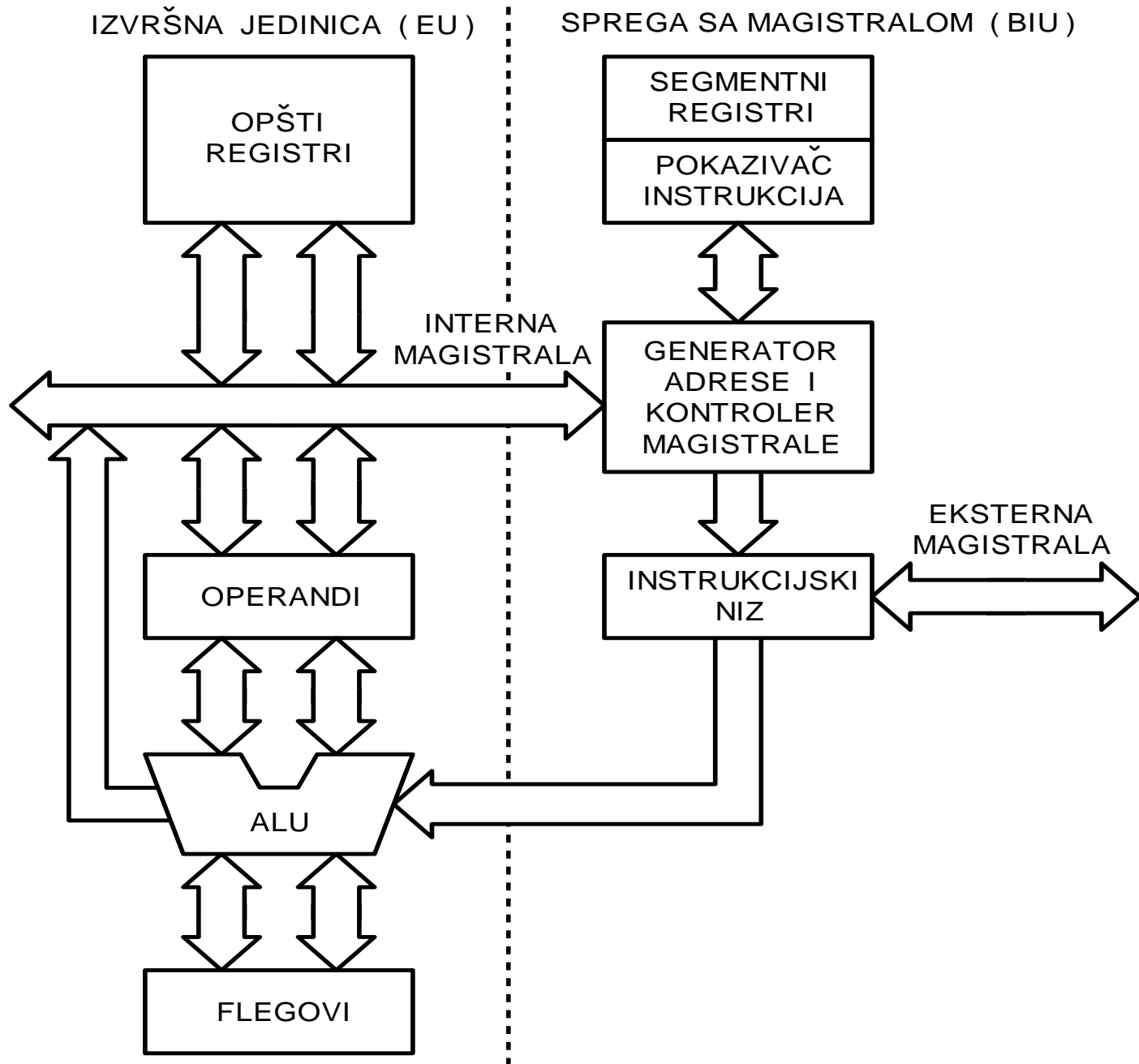
1. Izvršnu jedinicu

(EU - “*execution unit*”)

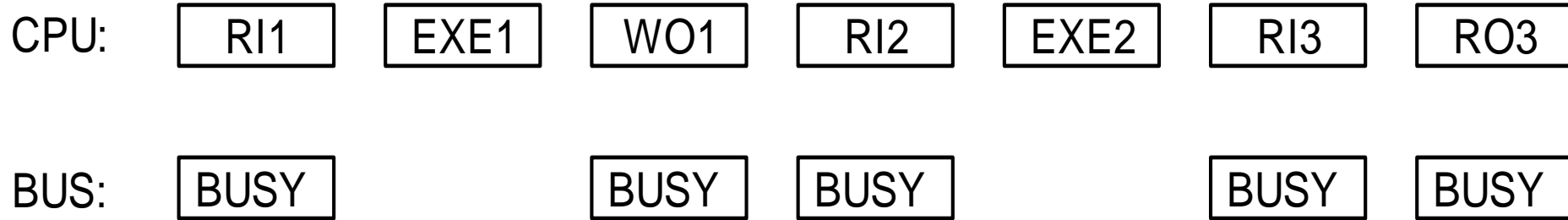
2. Jedinicu za spregu sa magistralom

(BIU - “*bus interface unit*”)

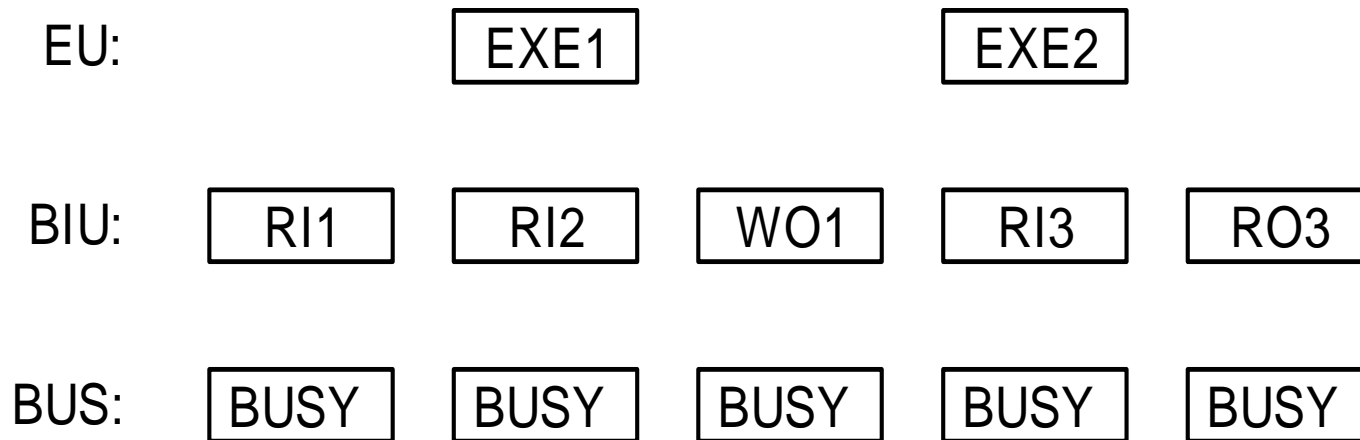
MIKROPROCESOR III GENERACIJE



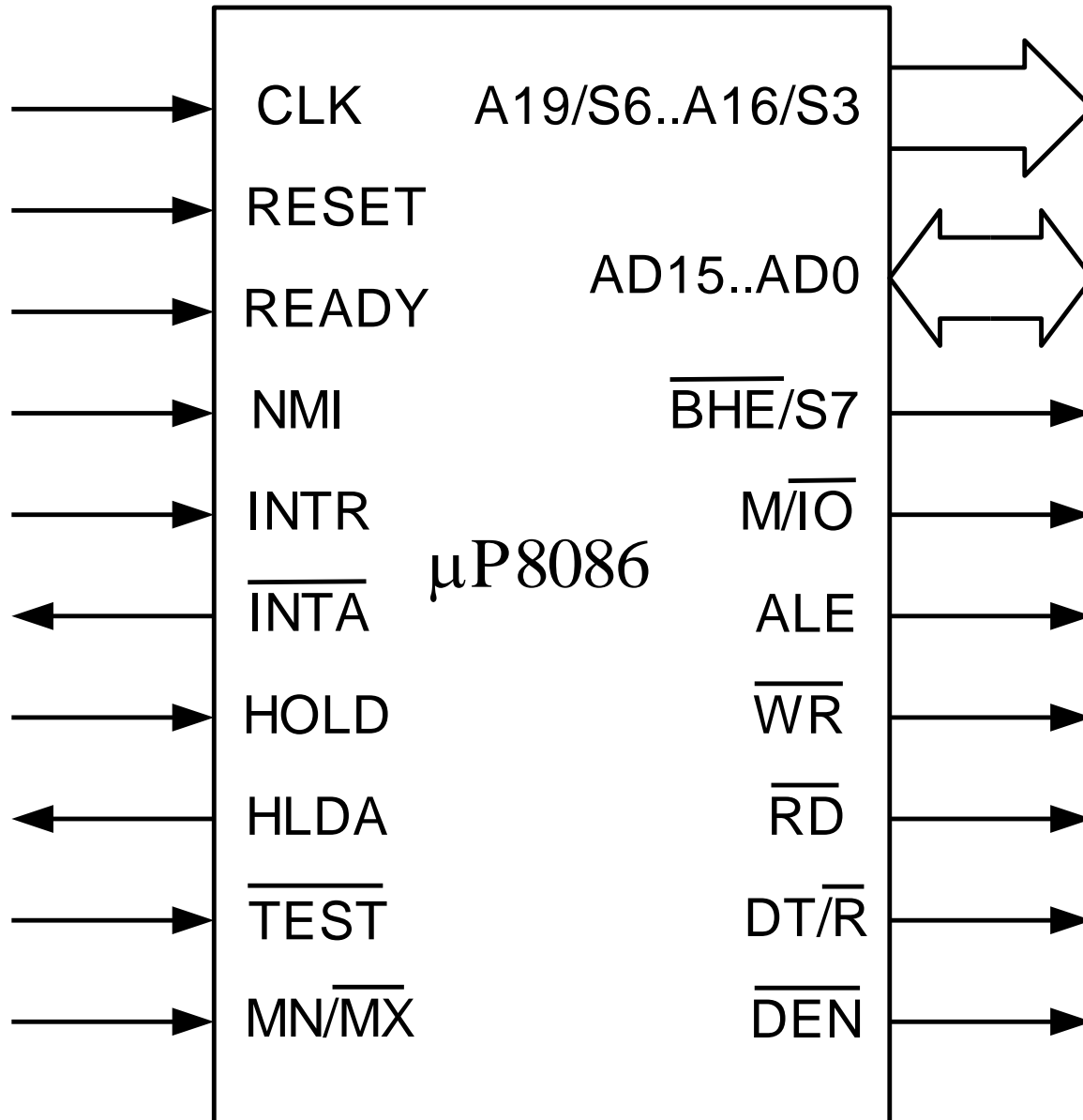
MIKROPROCESOR II GENERACIJE



MIKROPROCESOR III GENERACIJE



MIKROPROCESOR 8086



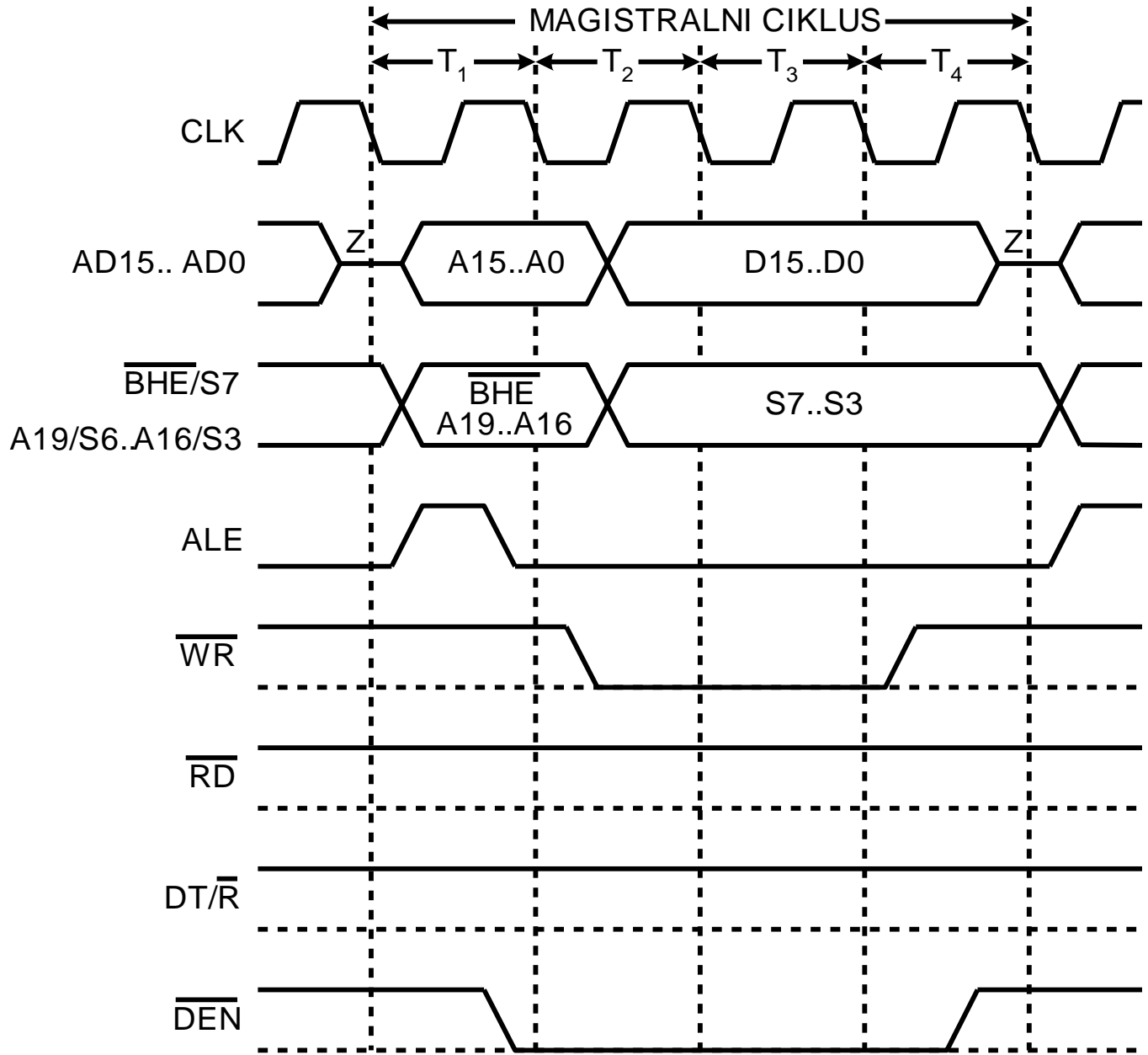
STATUSNI SIGNALI S3 I S4

S4	S3	Segmentni registar
0	0	ES
0	1	SS
1	0	CS ili nijedan
1	1	DS

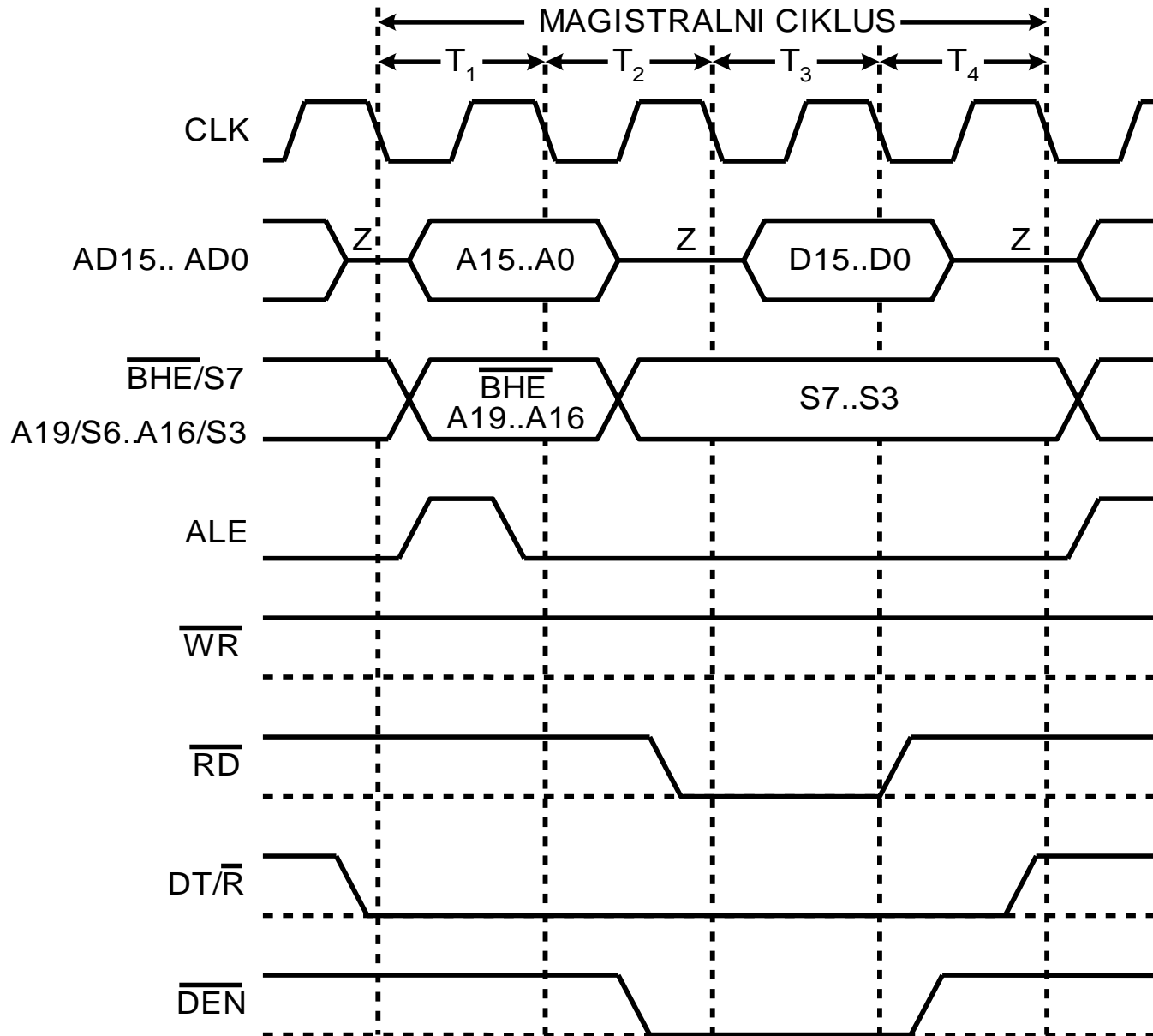
ADRESIRANJE REČI I BAJTOVA

BHE/	A0	PRISTUP
0	0	2-bajtna reč na parnoj adresi
0	1	Bajt na neparnoj adresi
1	0	Bajt na parnoj adresi
1	1	Ne koristi se

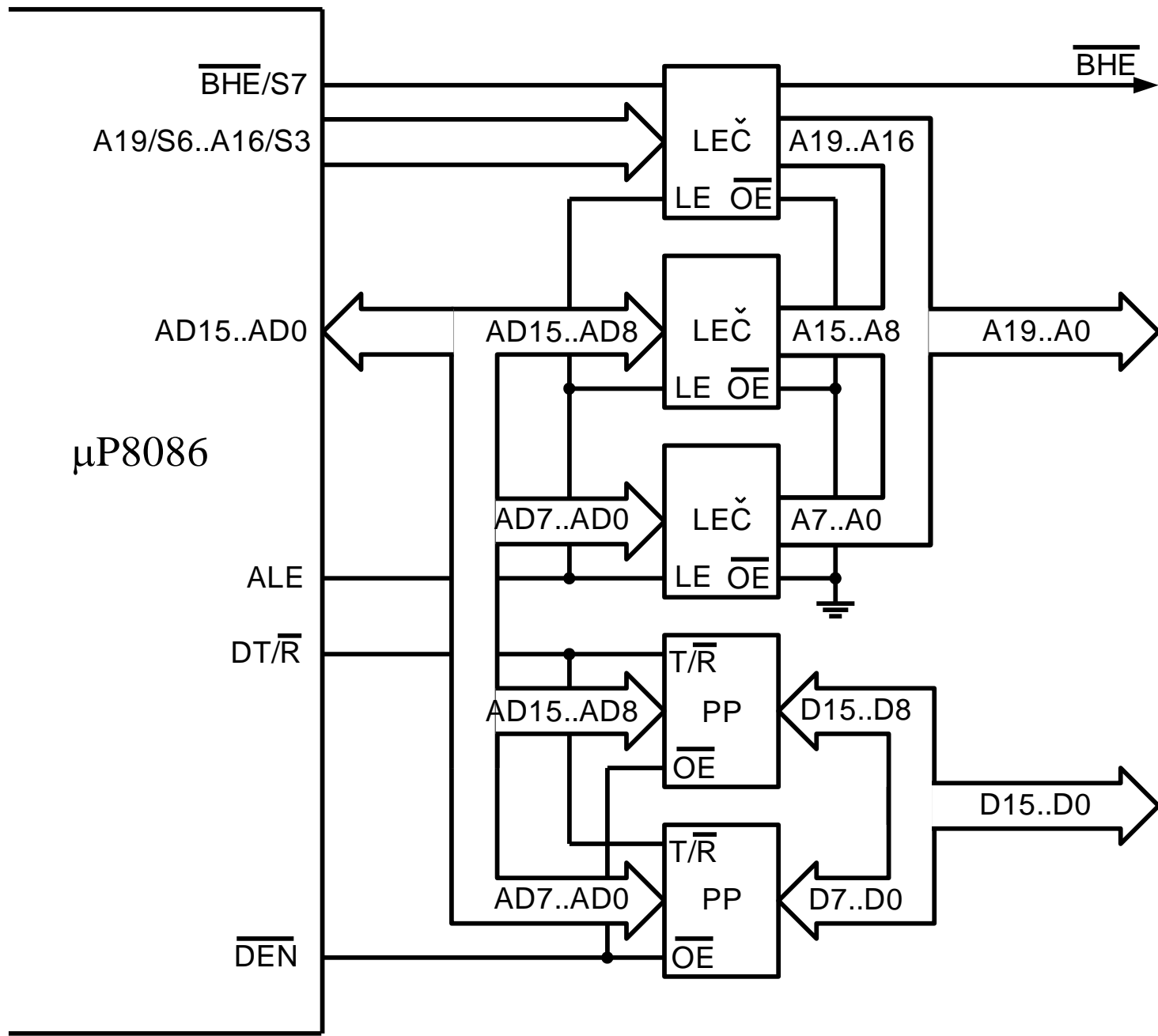
MAGISTRALNI CIKLUS UPISA



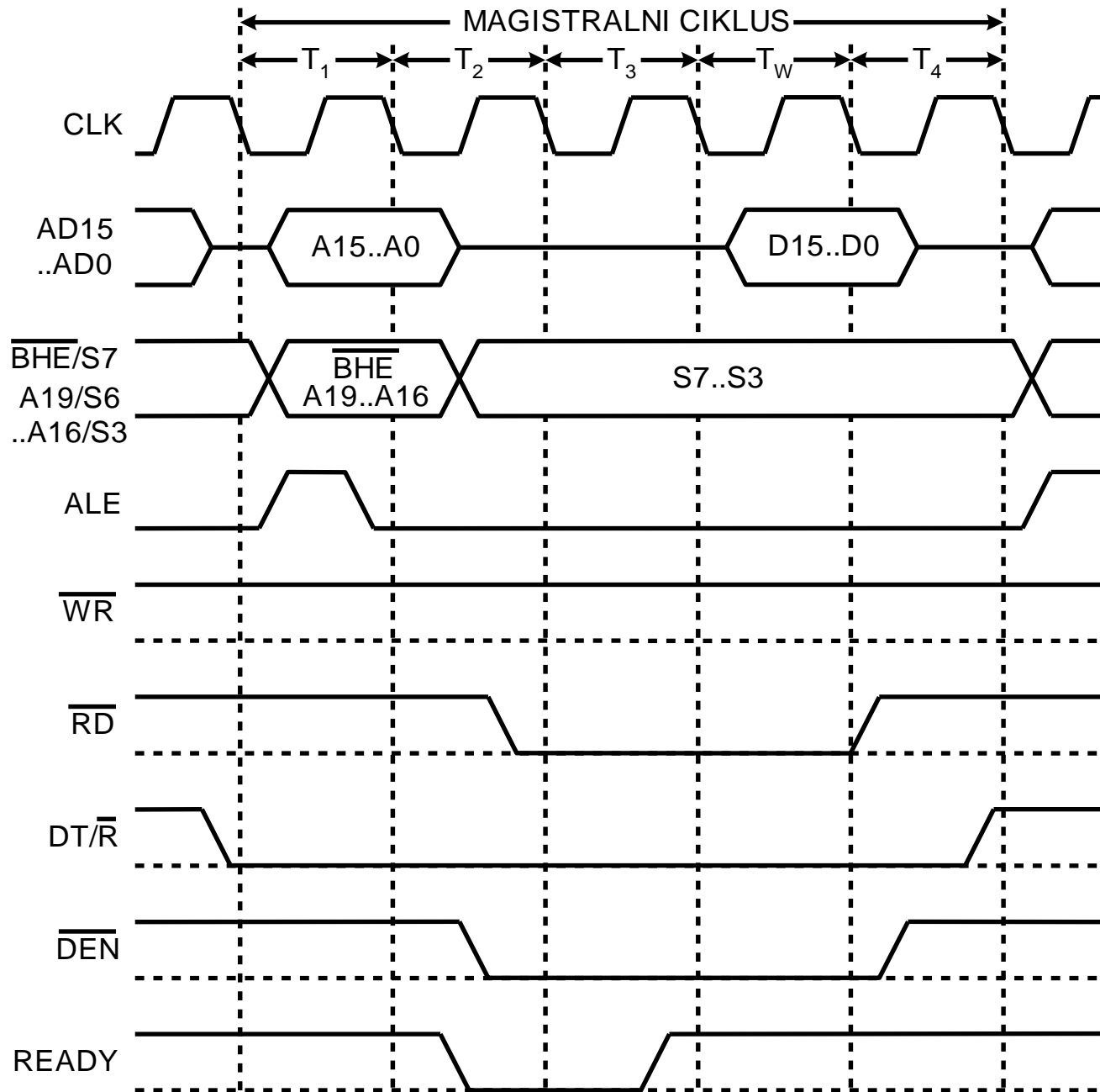
MAGISTRALNI CIKLUS ČITANJA



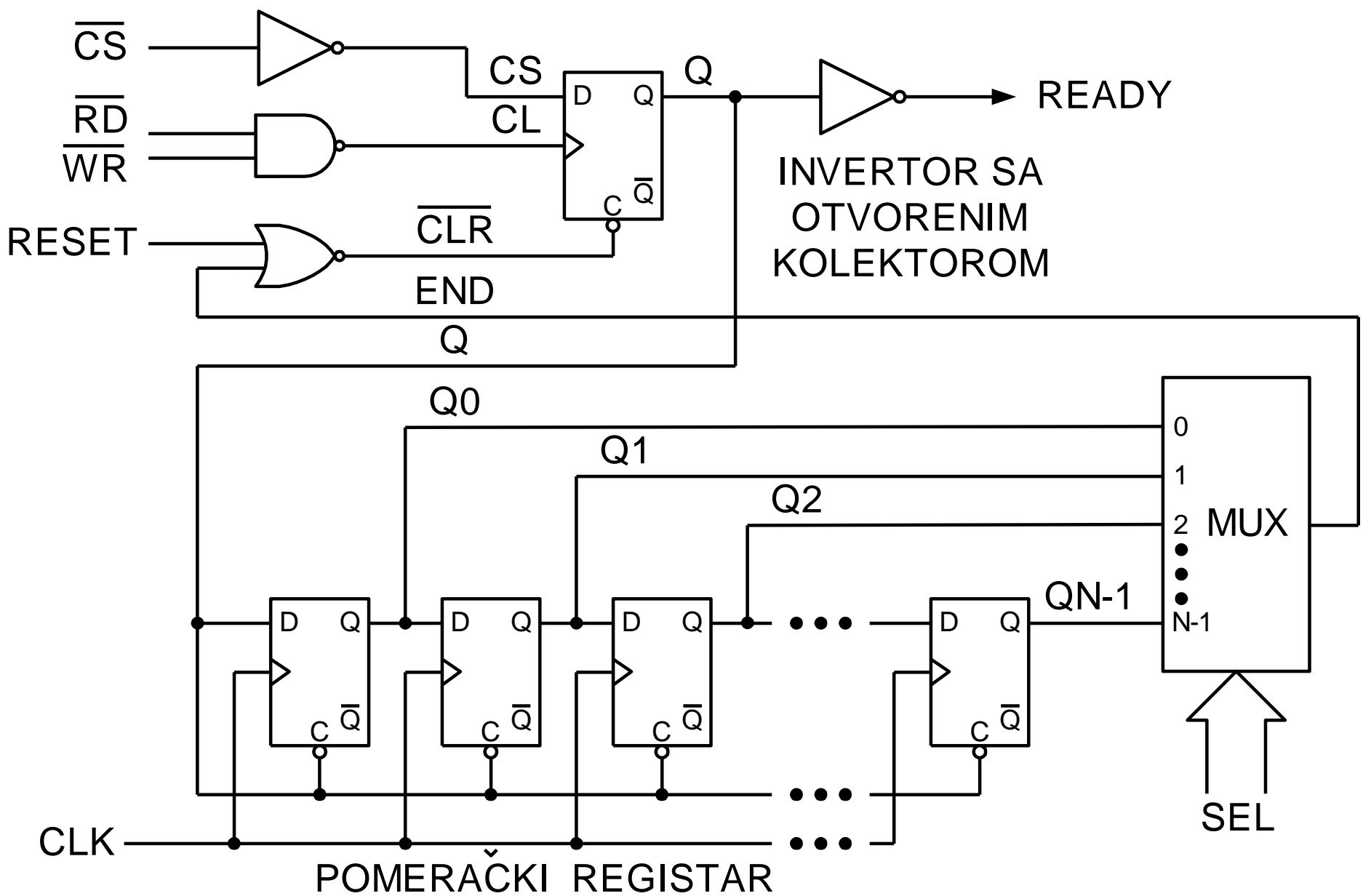
SPREGA SA MAGISTRALAMA



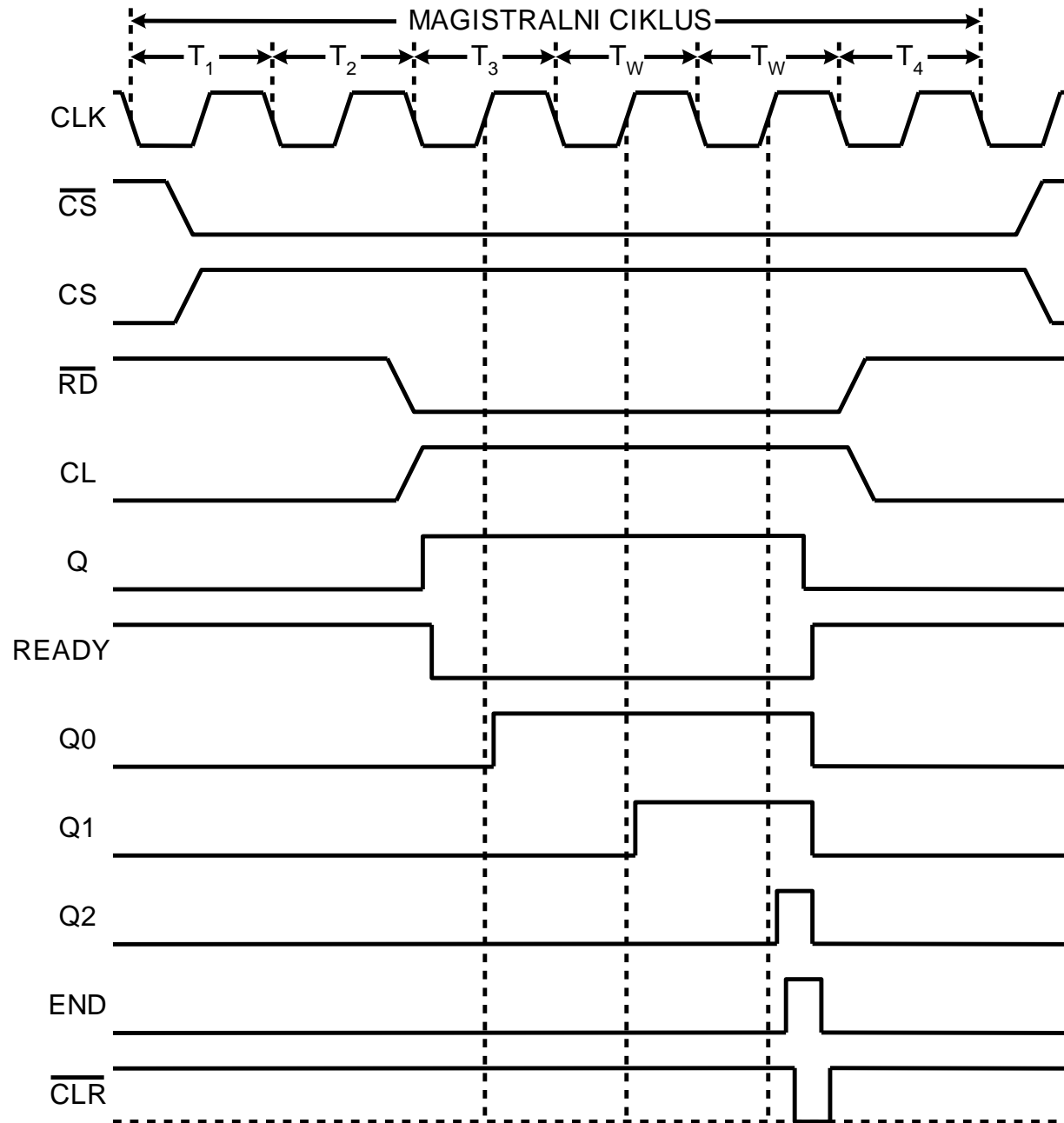
SIGNAL ČEKANJA READY



GENERATOR SIGNALA READY



DVA STANJA ČEKANJA



REGISTRI MIKROPROCESORA 8086

15 8 7 0

AH	AL
BH	BL
CH	CL
DH	DL

AX AKUMULATOR ("ACCUMULATOR")
 BX BAZNI REGISTRAR ("BASE REGISTER")
 CX BROJAČKI REGISTRAR ("COUNT REGISTER")
 DX REGISTRAR PODATAKA ("DATA REGISTER")

15 0

SP
BP
SI
DI

POKAZIVAČ STEKA ("STACK POINTER")
 POKAZIVAČ BAZE ("BASE POINTER")
 INDEKS IZVORIŠTA ("SOURCE INDEX")
 INDEKS ODREDIŠTA ("DESTINATION INDEX")

CS
SS
DS
ES

SEGMENTNI REGISTRAR PROGRAMA ("CODE SEGMENT")
 SEGMENTNI REGISTRAR STEKA ("STACK SEGMENT")
 SEGMENTNI REGISTRAR PODATAKA ("DATA SEGMENT")
 DODATNI SEGMENTNI REGISTRAR ("EXTRA SEGMENT")

15 0

IP

POKAZIVAČ INSTRUKCIJA ("INSTRUCTION POINTER")

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

				OF	DF	IF	TF	SF	ZF		AF		PF		CF
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PSW

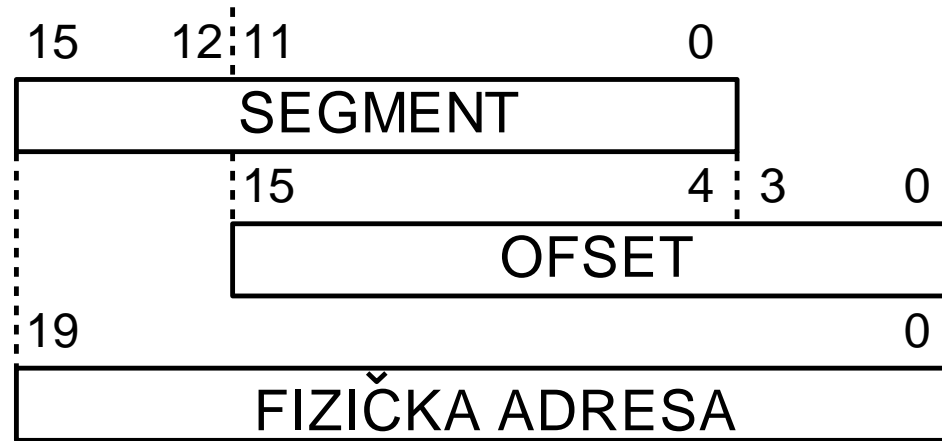
REGISTRAR FLEGOVA ("PROGRAM STATUS WORD")

FLEGOVI

- CF fleg prenosa (“*carry flag*”)
- PF fleg parnosti (“*parity flag*”)
- AF dodatni fleg (“*auxiliary flag*”)
- ZF fleg nultog rezultata (“*zero flag*”)
- SF fleg znaka (“*sign flag*”)
- TF fleg testiranja (“*trap flag*”)
- IF fleg dozvole maskiranog prekidnog zahteva (“*interrupt flag*”)
- DF fleg smeru promene adresa (“*direction flag*”)
- OF fleg prekoračenja (“*overflow flag*”)

FIŽIČKA ADRESA

fizička adresa = 16 x segment + offset



Segment	Ofset	Fizička adresa
CS	IP	Program
SS	SP	Stek
DS, CS, ES, SS	SI	Izvorište niza
ES	DI	Odredište niza
DS, CS, ES, SS	Opšti registri	Promenljive
SS, CS, DS, ES	BP + registri	Promenljive

16-BITNI STEK

- PRE SMEŠTANJA PODATKA NA STEK INSTRUKCIJOM PUSH POKAZIVAČ STEKA SP SE DEKREMENTIRA ZA 2.
- POSLE UZIMANJA PODATKA SA STEKA INSTRUKCIJOM POP POKAZIVAČ STEKA SP SE INKREMENTIRA ZA 2.

